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Ultra-fast 5 ns, Single Supply Comparators

Preliminary AD8561/8564

FEATURES

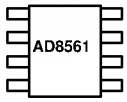
5 ns Propagation Delay
Single-Supply Operation
Low Power
Separate Input and Output Sections
Compatible with TTL and CMOS Logic
Wide Output Swing
Latch Function on Single

APPLICATIONS

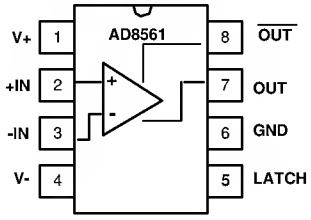
High Speed Timing
Line Receivers
High Speed V to F Converters
Battery Operated Instrumentation
High Speed Sampling
Window Comparators
Read Channel Detection

PIN CONFIGURATIONS

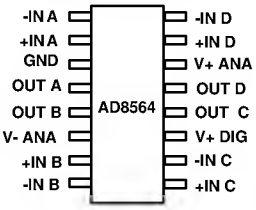
8-Lead Narrow-Body SO
(S Suffix)



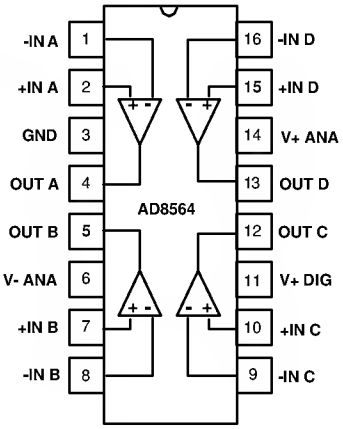
8-Lead Epoxy DIP
(P Suffix)



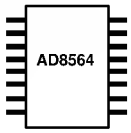
16-Lead Narrow-Body SO
(S Suffix)



16-Lead Epoxy DIP
(P Suffix)



16-Lead TSSOP
(RU Suffix)



GENERAL DESCRIPTION

The AD8561 and AD8564 are single and quad 5 ns comparators with separate input and output sections. Separate supplies enable the input stage to be operated from +5 volts to as high as ±5 volts.

Ultra fast 5 ns propagation delay makes the AD8561 and AD8564 the perfect choice for high timing circuits and line receivers. Independent analog and digital supplies provide excellent protection from supply pin interaction.

The AD8561 and 8564 are specified over the industrial (–40° to +85°C) temperature range. The single AD8561 is available in both the 8-pin plastic DIP or narrow SO-8 surface mount packages. The quad AD8564 is available in the 16-pin plastic DIP, narrow SO-16 surface mount, and 16-pin TSSOP packages.

REV. 0

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AD8561/8564 — SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_{CC} = V_{DD} = +5.0V, V_{EE} = 0V, T_A=+25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	3	mV
		-40°C ≤ T_A ≤ +85°C			4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0V			±4	µA
	I_B	-40°C ≤ T_A ≤ +85°C			±9	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			±3	µA
Input Common Mode Voltage Range	V_{CM}		0		+2.75	V
Common-Mode Rejection Ratio	CMRR	0V ≤ V_{CM} ≤ 2.75V	70	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{in}			3.0		pF
LATCH ENABLE INPUT (AD8561 only)						
Logic "1" Voltage Threshold	V_{IH}		2.0			V
Logic "0" Voltage Threshold	V_{IL}				0.8	V
Logic "1" Current	I_{IH}	V_{LH}=3.0V		1	20	µA
Logic "0" Current	I_{IL}	V_{LL}=0.3V		1	20	µA
Latch Enable						
Pulse Width	$t_{PW(E)}$			6		ns
Setup Time	t_S			2		ns
Hold Time	t_H			1		ns
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	I_{OH} = -3.2 mA, ΔV_{IN}>250mV	2.4	3.5		V
Logic "0" Voltage	V_{OL}	I_{OL} = 3.2 mA, ΔV_{IN}>250mV		0.3	0.4	V
DYNAMIC PERFORMANCE						
Propagation Delay	t_p	100 mV Step with 20 mV OD[1]		5	7	ns
		-40°C ≤T_A ≤ +85°C[1]			9	ns
Propagation Delay	t_p	100 mV Step with 5 mV OD[1]		8	10	ns
Differential Propagation Delay	Δt_p	100 mV Step with 20 mV OD[1]		0.5	2.0	ns
Rise Time		20% to 80%		3		ns
Fall Time		20% to 80%		3		ns
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	+4.5 ≤ V_{CC} & V_{DD} ≤ + 5.5V		80		dB
Analog Supply Current/Comparator	I_{CC}			2.3	3.5	mA
		-40°C ≤T_A ≤ +85°C			3.9	mA
Digital Supply Current/Comparator	I_{DD}	V_O = 0V, R_L = ∞		1.5	1.75	mA
		-40°C ≤T_A ≤ +85°C			2.0	mA
Analog Supply Current/Comparator	I_{EE}			2.3	3.5	mA
		-40°C ≤T_A ≤ +85°C			3.9	mA

[1] Guaranteed by design.

AD8561/8564 — SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_{CC} = V_{DD} = +5.0V, V_{EE} = -5V, T_A=+25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	3	mV
		-40°C ≤T_A ≤ +85°C			4	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
Input Bias Current	I_B	V_{CM} = 0V			±4	µA
		-40°C ≤T_A ≤ +85°C			±9	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			±3	µA
Input Common Mode Voltage Range	V_{CM}		-4.9		+3.5	V
Common-Mode Rejection Ratio	CMRR	-5.0V ≤ V_{CM} ≤ 2.75V	70	85		dB
Large Signal Voltage Gain	A_{VO}	R_L = 10 kΩ		3000		V/V
Input Capacitance	C_{IN}			3.0		pF
LATCH ENABLE INPUT (AD8561 only)						
Logic "1" Voltage Threshold	V_{IH}		2.0			V
Logic "0" Voltage Threshold	V_{IL}				0.8	V
Logic "1" Current	I_{IH}	V_{LH}=3.0V		1	20	µA
Logic "0" Current	I_{IL}	V_{LL}=0.3V		1	20	µA
Latch Enable						
Pulse Width	$t_{PW(E)}$			6		ns
Setup Time	t_S			1.5		ns
Hold Time	t_H			0.8		ns
DIGITAL OUTPUTS						
Logic "1" Voltage	V_{OH}	I_{OH} = -3.2 mA	2.6	3.6		V
Logic "0" Voltage	V_{OL}	I_{OL} = 3.2 mA		0.2	0.3	V
DYNAMIC PERFORMANCE						
Propagation Delay	t_p	100 mV Step with 20 mV OD[1]		6	8	ns
		-40°C ≤T_A ≤ +85°C		8	10	ns
Propagation Delay	t_p	100 mV Step with 5 mV OD[1]		8	10	ns
Differential Propagation Delay	Δt_p	100 mV Step with 20 mV OD[1]		0.5	2	ns
Rise Time		20% to 80%		3		ns
Fall Time		20% to 80%		3		ns
Dispersion		see Figure x				
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	± 4.5 ≤ V_{CC} & V_{EE} ≤ ± 5.5V	60	70		dB
Analog Supply Current/Comparator	I_{CC}			2.3	3.5	mA
		-40°C ≤T_A ≤ +85°C			3.9	mA
Digital Supply Current/Comparator	I_{DD}	V_O = 0V, R_L = ∞		0.9	1.1	mA
		-40°C ≤T_A ≤ +85°C			1.4	mA
Analog Supply Current/Comparator	I_{EE}			2.3	3.5	mA
		-40°C ≤T_A ≤ +85°C			3.9	mA

[1] Guaranteed by design.

ELECTRICAL SPECIFICATIONS (@ V_{CC}= V_{DD} = +3.0V, V_{EE} = 0V, T_A=+25°C unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}				4.5	mV
Input Common Mode Voltage Range	V_{CM}		0		+1.8	V
Common-Mode Rejection	CMRR	$0.1V \le V_{CM} \le 1.8V$	65			dB
OUTPUT CHARACTERISTICS						
Output High Voltage	V_{OH}	I_{OH} = -3.2 mA, V_{IN}>250mV	2.1			V
Output Low Voltage	V_{OL}	I_{OL} = 3.2 mA, V_{IN}>250mV			0.25	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$+2.7 \le V_{CC}, V_{EE} \le +6V$	60			dB
Analog Supply Current/Comparator	I_{ANA}			2.2	3.1	mA
Digital Supply Current /Comparator	I_{DIG}	V_O = 0V, R_L = ∞		0.8	1.0	mA
DYNAMIC PERFORMANCE						
Propagation Delay	t_p	100 mV Step with 20 mV OD[1]		7		ns

[1] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Total Analog Supply Voltage.....+16 V
Digital Supply Voltage.....+16 V
Analog Positive Supply - Digital Positive Supply .....-600 mV
Input Voltage[1].....±7 V
Differential Input Voltage .....±8 V
Output Short-Circuit Duration to Gnd.....Indefinite
Storage Temperature Range
N, R Package.....-65°C to +150°C
Operating Temperature Range
AD8561, AD8564.....-40°C to +85°C
Junction Temperature Range
N, R Package.....-65°C to +150°C
Lead Temperature Range (Soldering, 10 sec).....+300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
8-Pin Plastic DIP (N)	103	43	°C/W
8-Pin SO (R)	158	43	°C/W
16-Pin Plastic DIP (N)	90	47	°C/W
16-Pin SO (R)	113	37	°C/W
16-Pin TSSOP (RU)	180	37	°C/W

NOTES

[1] The analog input voltage is equal to ±7 volts or the analog supply voltage, whichever is less.

[2] θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for , P-DIP, and θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8561AN	-40°C to +85°C	8-Pin Plastic DIP	N-8
AD8561AR	-40°C to +85°C	8-Pin SOIC	SO-8
AD8564AN	-40°C to +85°C	16-Pin Plastic DIP	N-16
AD8564AR	-40°C to +85°C	16-Pin SOIC	SO-16
AD8564ARU	-40°C to +85°C	16-Pin TSSOP	RU-16